THEJAS32

High performance, RISC-V based 32-bit MCU with 256KB SRAM, 3 UART, 4 SPI, 3 I2C, 8 PWM, 3 TIMERS and 32 GPIO interfaces

Features

- Core: VEGA 32 bit ET1031 CPU
  - RISC-V (RV32IM) CPU
  - 100MHz maximum frequency,
  - 1.3 DMIPS/MHz (Dhrystone 2.1)
  - 3.33 CoreMark/MHz
  - Hardware multiplication and Division
- Memories
  - 256KB of SRAM
  - External SPI Flash support
- Clock, reset and supply management
  - I/O voltage -3.3 V
  - Core voltage -1.2V
  - External oscillator 50-100 MHz
  - DC Current per I/O Pin-12mA
- Operating temperature 0 to +70 °C
- 32 I/O Ports
  - 32 General purpose 3.3 V tolerant I/Os
  - 12 I/O ports with interrupt capability
- 3 UART
  - Programmable word length, stop bits and parity
  - 5/ 6/ 7 or 8-bit character
  - Even, odd, or no-parity bit
  - 1, 1$_{1/2}$, or 2 stop bits.
  - Programmable baud rate
- 4 SPI
  - Full-duplex synchronous serial operation
  - Programmable clock rate
  - Double-buffered data register
  - Programmable polarity and phase
  - 8 to 16-bit frames
  - MSB-first and LSB-first frames
- 3 I2C
  - Configurable SCK frequency
  - Separate Receive/Transmit FIFO
  - Fully configurable interrupt for Receive/Transmit.
  - Auto STOP generation while detecting NACK condition on the bus

LQFP128 14 x 14 mm

- 8 PWM
  - Separate interrupt enable/disable for each channel
  - 32-bit Period counter and ON/OFF counter
  - Right aligned and left aligned PWM signals.
  - Support for one shot and continuous mode of operation.
  - Separate control bits for each channel
- 3 Timers
  - 32-bit programmable timers
  - Support for two operating modes: free-running and user-defined count
- Interrupt Controller
  - Active high interrupts
- Applications
  - Sensor fusion
  - Smart metering
  - Wearable devices
  - Low power IoT
  - System supervisors
  - Remote sensors
  - Toy and electronic education equipments
  - Legacy 8/16 –bit applications
  - Industrial networking
  - Motor drives
  - GPS platforms
  - PLCs
  - Inverters

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1. Introduction

This document provides mechanical device characteristics of the THEJAS32SoC. THEJAS32 is a low-power SoC for robust embedded applications. For more details on the whole Vega microprocessors family, refer to www.vegaprocessors.in/index.php
For information on programming please refer to the THEJAS32 Flash Programming Manual.

2. Description

The THEJAS32 SoC integrates the power of the VEGA ET1031 32-bit single-core in-order, 3-stage pipeline processor, with various communication and peripheral interfaces in an LQFP 128 package. The THEJAS32 SoC operates at a frequency of 100MHz. It includes the VEGA ET1031 microprocessor, 256KB internal SRAM, three UARTs, four SPIs, three timers, eight PWMs, three I2C interfaces, and 32 GPIOs. The processor core is based on the open-source RISC-V Instruction Set Architecture . This SoC is designed and developed by the Centre for Development of Advanced Computing (C-DAC) as part of the Digital India RISC-V (DIR-V) Program, by the Ministry of Electronics and Information Technology, Government of India.

The device operates on a 3.3V power supply. They are available in the 0 to +70°C temperature range. These features make the THEJAS32 SoC suitable for a wide range of applications such as sensor fusion, smart meters, system supervisors, remote sensors, small IoT devices, wearable devices, motor drives, etc.

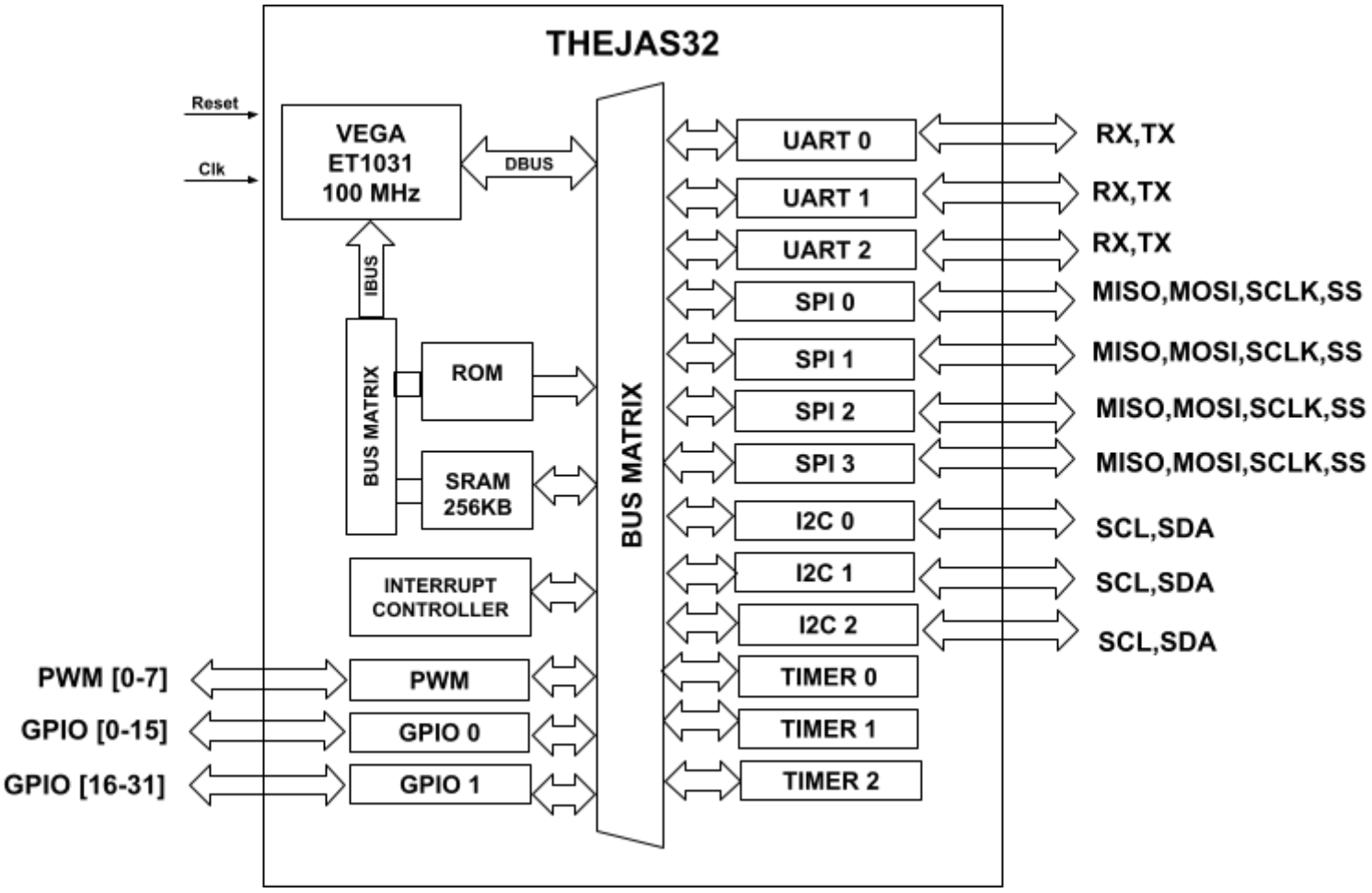
2.1. Device overview

The description below gives an overview of the complete range of peripherals.

Table 1. THEJAS32 device features and peripherals

THEJAS32 SoC Peripherals	
SRAM	256KB
General purpose I/O	32
PWM	8
Timers	3
SPI	4
I2C	3
UART	3
CPU frequency	100MHz
I/O voltage	3.3V
Core Voltage	1.2V
Operating temperatures	0 to +70 °C
Packages	LQFP 128

Figure 1. THEJAS32 SoC block diagram



2.2. Overview

2.2.1. VEGA ET1031 – CPU

ET1031 is a 32-bit three stage pipeline processor well suited for low power embedded applications.

- 32-bit RISC-V(RV32IM)Instruction Set Architecture
- 3-stage In-Order pipeline
- Support for privileged Instruction set
- 32-bit load/store architecture
- Pipelined Harvard architecture
- Byte, half-word and word memory access
- Software Interrupt support
- Timer Interrupt support
- External Interrupt support
- Processor Modes – Machine

2.2.2. Embedded SRAM

256KB of embedded SRAM accessed (read/write) at CPU clock speed.

2.2.3. Clock

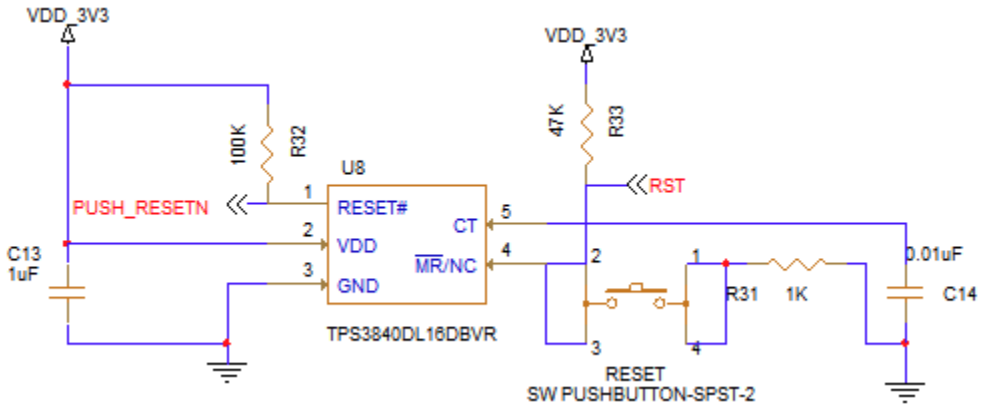
The CLK pin of the device is furnished with an external 100MHz clock signal, with the recommended part number being **SIT8008AC-33-33E-100.000000.**

2.2.4. Reset

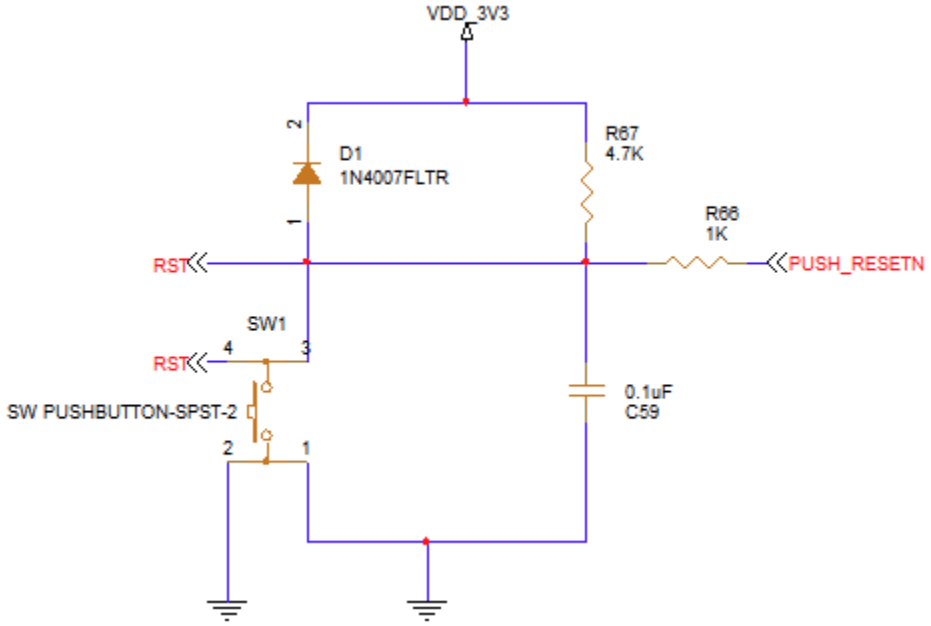
Reset is active low. An active low pulse on PUSH_RESETN with a minimum period of 100 ns will reset the device.

Figure 2 : Typical reset circuits

- With Reset IC (TPS3840DL16DBVR)



- Without Reset IC



2.2.5. Boot modes

At startup, boot pins (BOOT_SEL) are used to select one of two boot options:

- Default - UART Mode

  A program binary can be transferred using the XMODEM protocol on UART 0.

- SPI Flash Mode

  The bootloader transfers the initial 250KB of data from the flash memory connected to SPI 3 into the SRAM and then jumps to the program. For further information on programming, please refer to the *THEJAS32 Flash Programming Manual*.

The boot pin (BOOT_SEL) facilitates the programming of the Flash memory via UART, wherein a high state sets the default UART mode, while a low state activates the SPI Flash mode.

Note: Baud Rate settings

For default UART mode boot, It is mandatory to set the UART 0 baud rate using seven general purpose input/output (GPIO) pins, GPIO 25 to 31. The baud rate calculation is given below

BAUD RATE = FREQUENCY/(16*115200)

The table below provides the baud rate settings for a frequency of 100MHz.

BAUD RATE = 100MHz / (16*115200) =100000000/1843200 = 54 (binary : 0110110)

GPIO	31 (MSB)	30	29	28	27	26	25(LSB)
ASSIGNED VALUE	0	1	1	0	1	1	0

Figure 3. Baud Rate for 100MHz typical application circuit

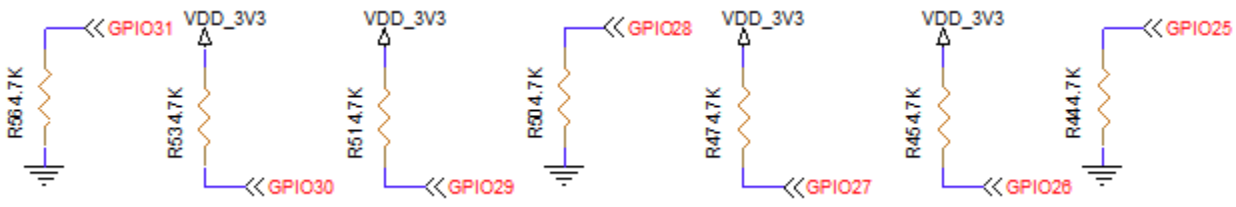


Figure 4. Typical application circuit for UART to USB

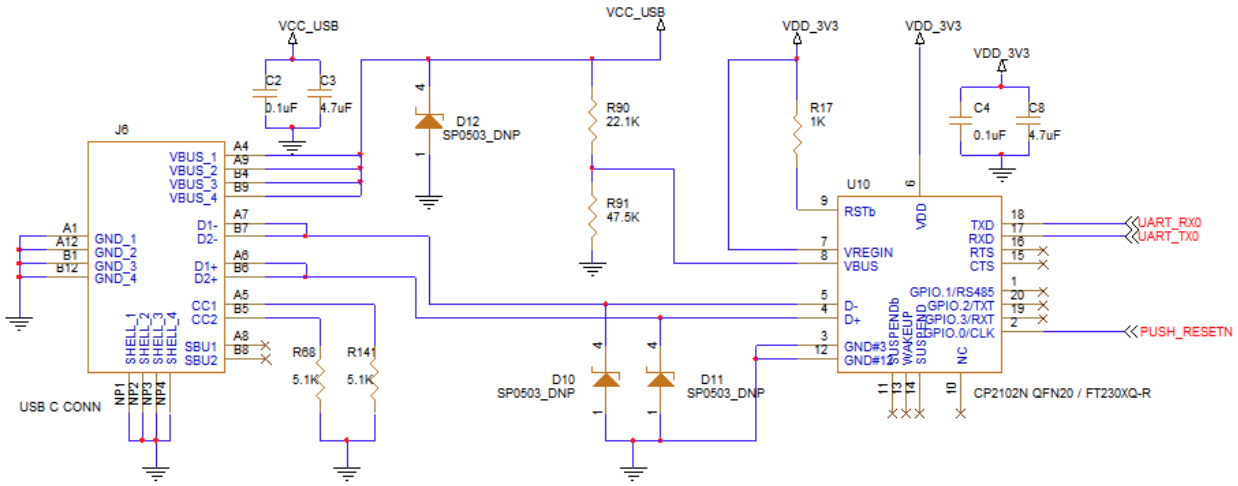
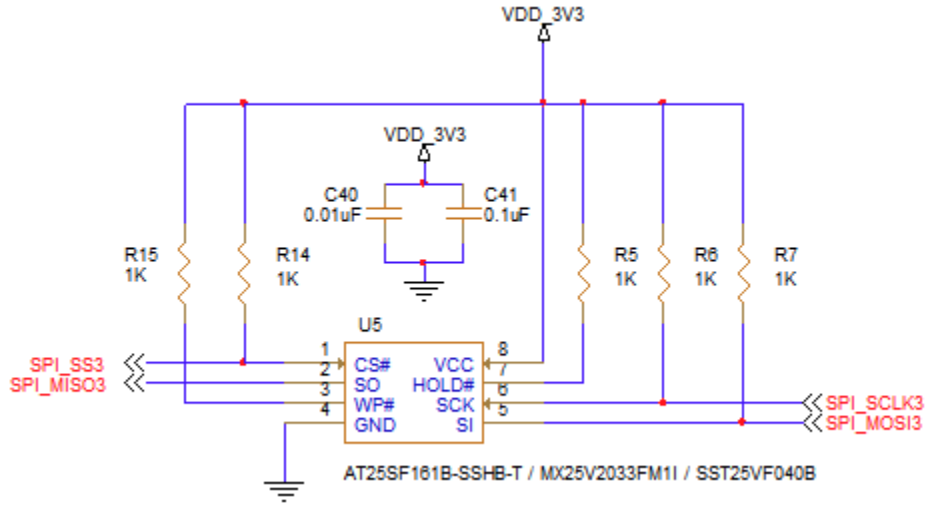


Figure 5. Typical application circuit for SPI Flash memory



2.2.6. Power supply schemes

V_{DDIO} = 3.3 V, External power supply for I/Os provided externally through V_{DDIO} pins.
V_{DD} = 1.2 V, External power supply for core provided externally through V_{DD} pins.

Table 2. THEJAS32 SoC Decoupling capacitors

It is recommended to incorporate decoupling capacitors of 0.1uF, 0.01uF and 10uF on each supply line to maintain stable voltage levels and minimize noise interference.The following table lists the requirements of all decoupling capacitors for the THEJAS32 device.

Pin Name	Ceramic		
	0.1uF	0.01uF	10uF
V_{DD}	5	6	3
V_{DDIO}	5	6	3

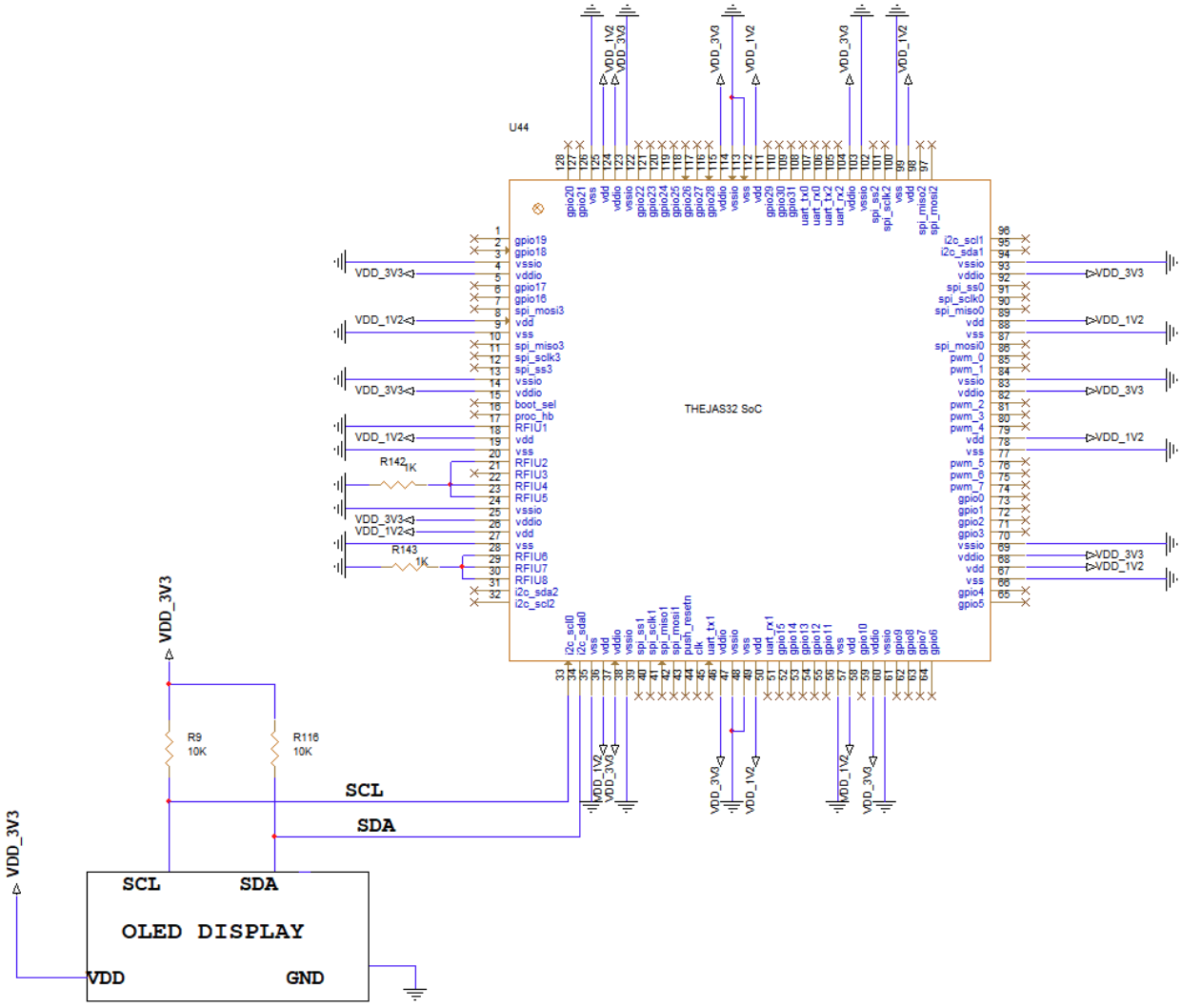
2.2.7. I2C

This device exclusively supports I2C master mode, a configuration where it acts as the initiator of data transfers on the bus, generating clock signals to facilitate communication. In this setup, other devices on the bus are recognized as slaves, responding to commands and data sent by the master. Pull-up resistors, typically set at 10KΩ, are necessary on both the SDA and SCL lines to ensure proper signal integrity and voltage levels in the I2C-bus communication system.

Routing guideline: I2C Length Matching (SDA>SCL)

- SDA0 should be 1.5367 mm greater than SCL0
- SDA2 should be 135.8 mm greater than SCL2

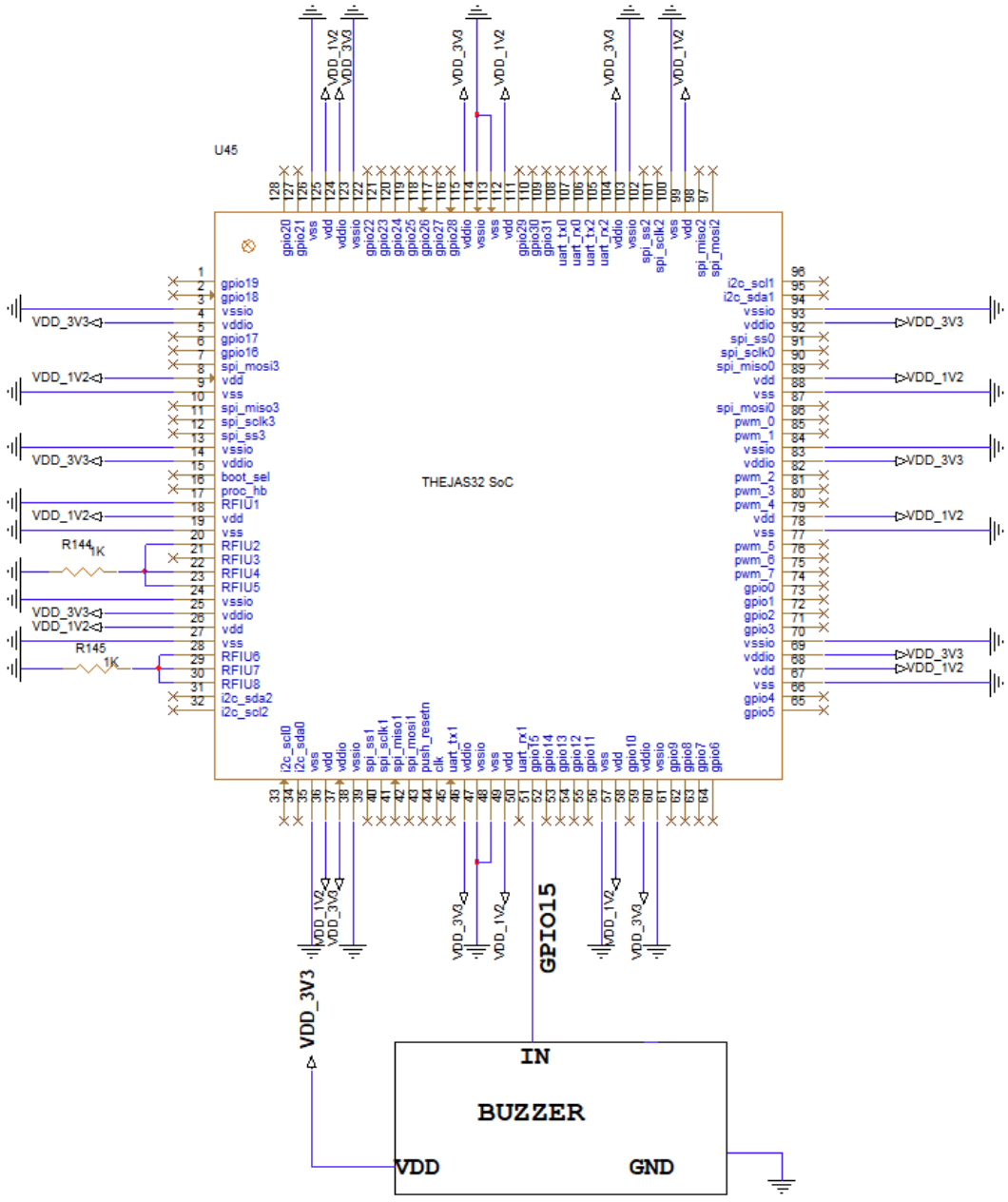
Figure 6. I2C typical application circuit



2.2.8. GPIO - general purpose inputs/outputs

The GPIO pins are configurable as either inputs or outputs. In output mode, an internal register governs the state of the output pin, while in input mode, the state of input pins is discernible by reading an internal register. Bit masking is supported in both read and write operations. Following system reset, GPIO lines revert to input mode as a default setting.

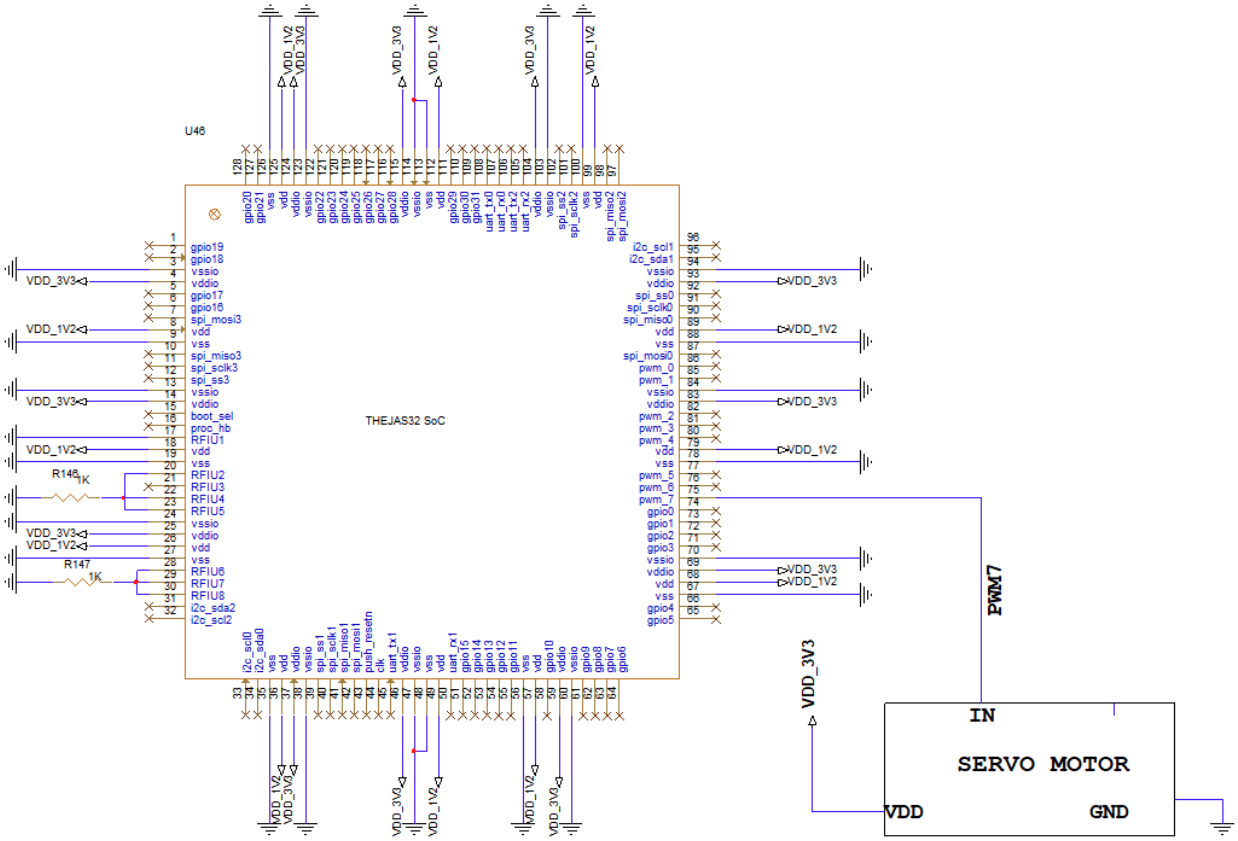
Figure 7. GPIO typical application circuit



2.2.9. PWM - Pulse width modulator

PWM controller provides eight individually programmable PWM Outputs.This PWM controller offers full programmability, enabling effortless customization of the output waveform. With a 32-bit Period counter and ON/OFF counter, it facilitates precise shaping of the PWM signal. Moreover, it supports the generation of both right-aligned and left-aligned PWM signals, and seamlessly toggles between one-shot and continuous operating modes.

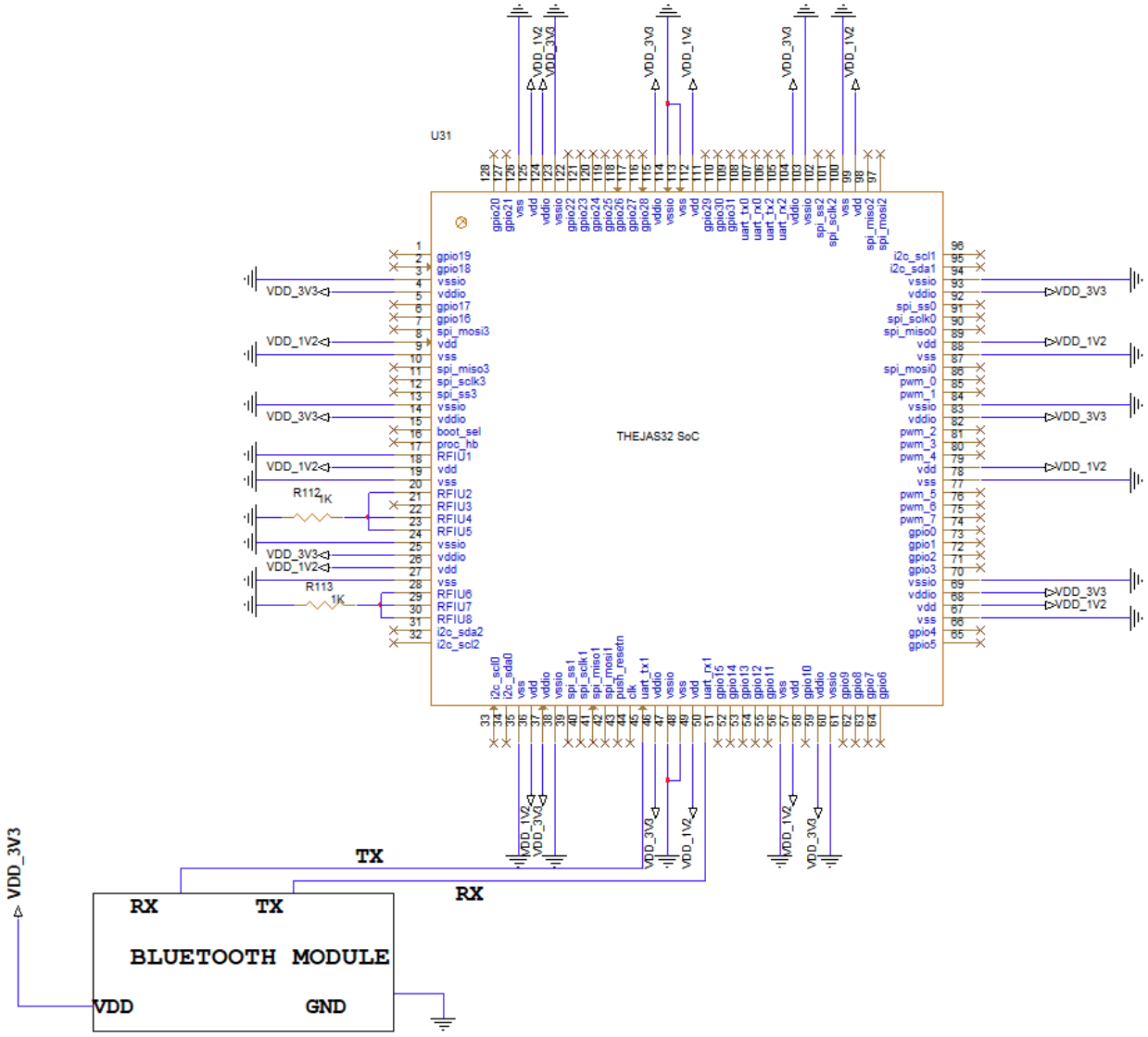
Figure 8. PWM typical application circuit



2.2.10. UART - Universal Asynchronous Receiver/Transmitter

This device includes three UART's. The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to (2^{16}-1) and producing a 16X clock for driving the internal transmitter logic. Interrupts can be programmed to the user's requirements.

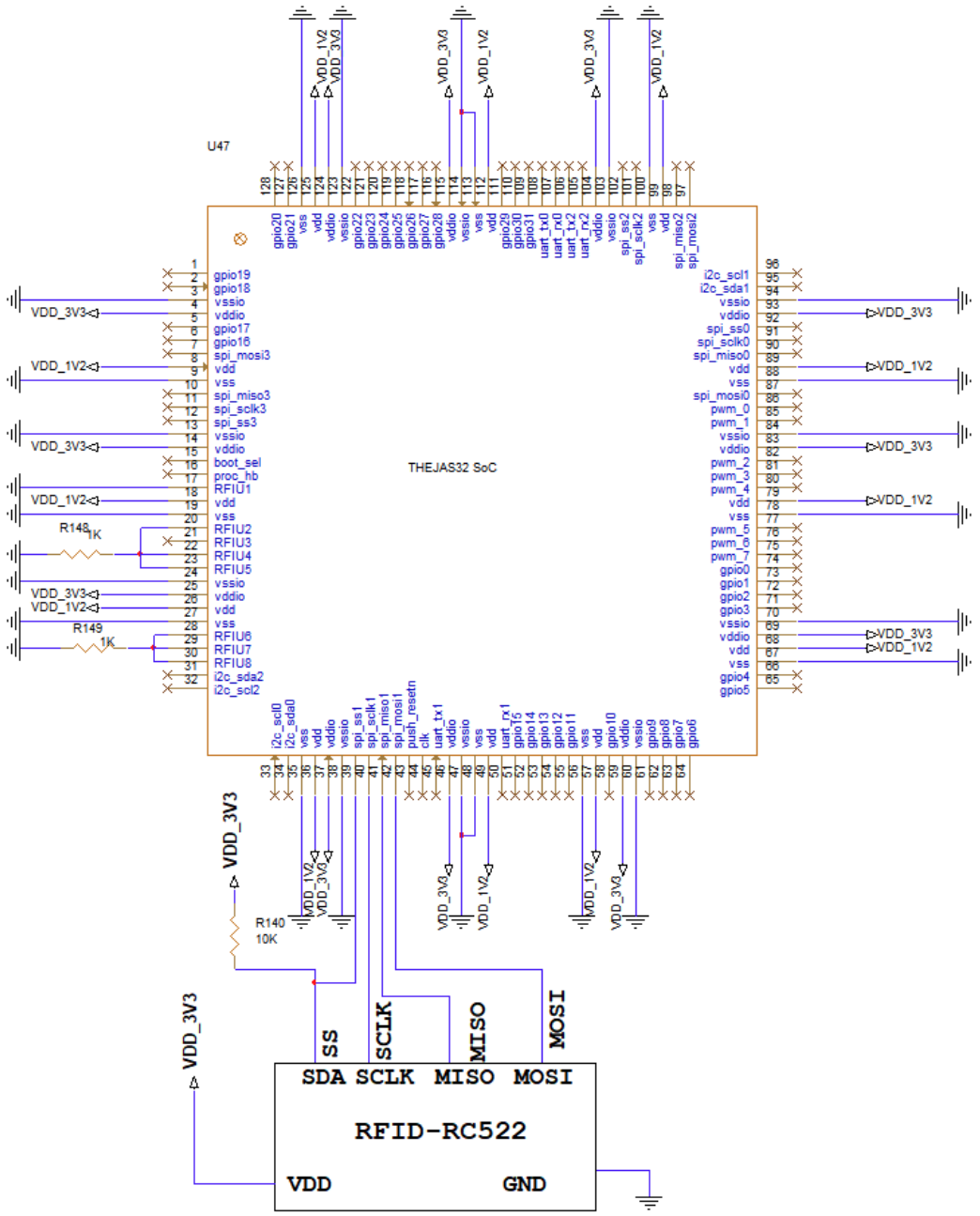
Figure 9. UART typical application circuit



2.2.11. SPI - Serial Peripheral Interface controller

This SPI controller facilitates master mode for both full duplex and simplex synchronous serial communication. It offers adjustable clock rates, enabling seamless integration with different devices. With double-buffered data registers and customizable polarity and phase configurations, it ensures adaptable data management. It supports frame sizes ranging from 8 to 16 bits and accommodates both MSB-first and LSB-first formats, providing versatility in data handling.

Figure 10. SPI typical application circuit



2.2.12. TIMER

The TIMER implements three identical but separately programmable timers. Timers count down from a programmed value and generate an interrupt when the count reaches zero. The width of the timer is 32 bits. Supports both free-running and user-defined count modes.

2.2.13. Interrupt controller

The interrupt controller comprises 32 level detector lines designed for generating interrupt requests, with each line independently maskable. A pending register tracks the status of interrupt requests. Also, it connects GPIO0 to GPIO11 to interrupt 10 to 22.

3. Pinout and pin descriptions

Figure 11. THEJAS32 SoC LQFP128 pinout

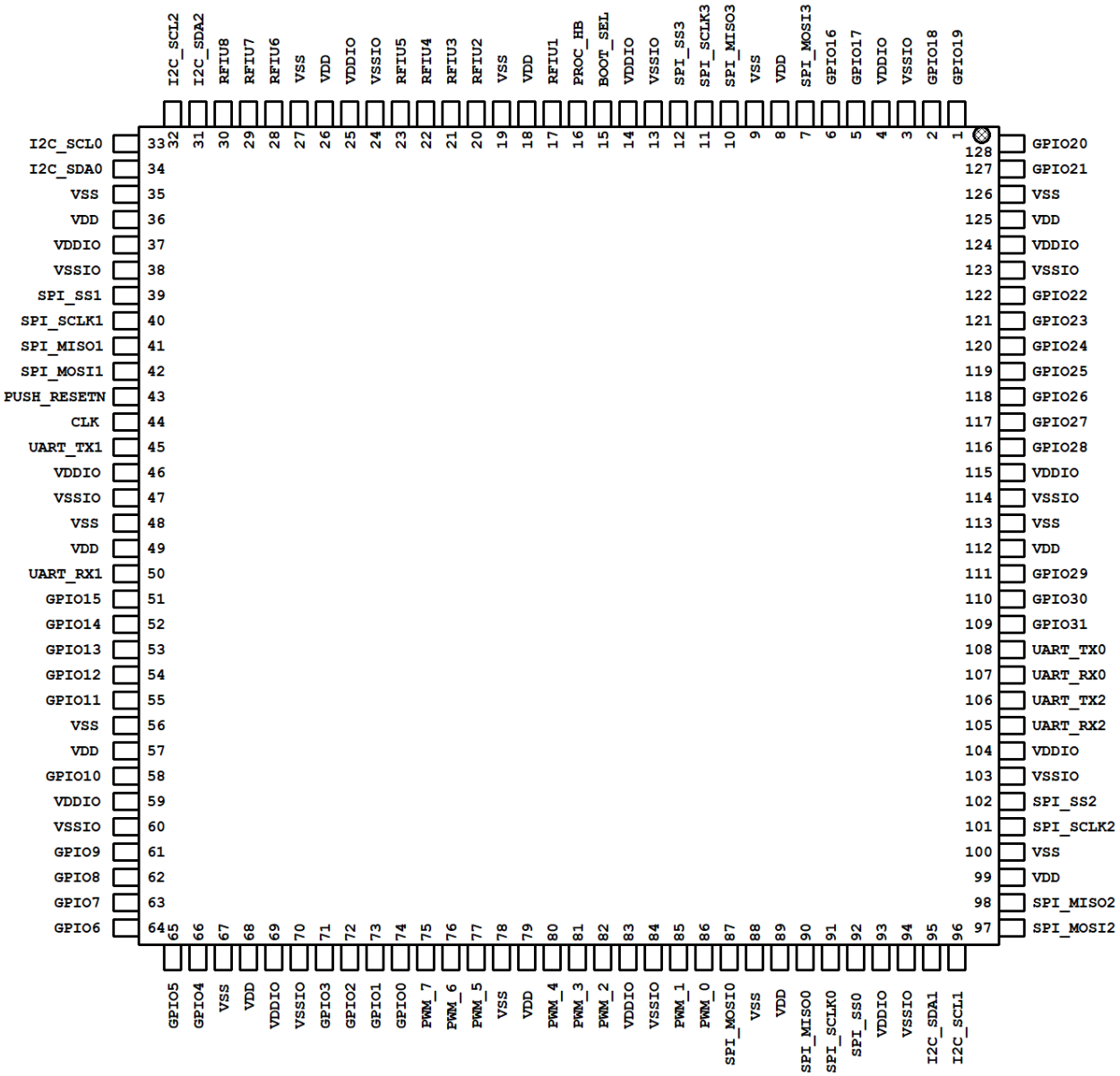


Table 3. THEJAS32 SoC pin definitions

Pin #	Pin Name	Pin Description	Type
1	GPIO19	General purpose IO GPIO1(3).	I/O
2	GPIO18	General purpose IO GPIO1(2).	I/O
3	VSSIO	Ground reference for IO pins.	S
4	VDDIO	Positive supply for IO pins. Connect to 3.3V supply.	S
5	GPIO17	General purpose IO GPIO1(1).	I/O
6	GPIO16	General purpose IO GPIO1(0).	I/O
7	SPI_MOSI3	SPI 3 Master Out Slave In.	O
8	VDD	Positive supply for logic. Connect to 1.2V supply.	S
9	VSS	Ground reference for logic.	S
10	SPI_MISO3	SPI 3 Master In Slave Out.	I
11	SPI_SCLK3	SPI 3 Clock.	O
12	SPI_SS3	SPI 3 Chip Select.	O
13	VSSIO	Ground reference for IO pins.	S
14	VDDIO	Positive supply for IO pins. Connect to 3.3V supply.	S
15	BOOT_SEL	Boot select.	I
16	PROC_HB	Heartbeat signal.	O
17	RFIU1	Connect to GND.	NA
18	VDD	Positive supply for logic. Connect to 1.2V supply.	S
19	VSS	Ground reference for logic.	S
20	RFIU2	Connect to GND through a 1K resistor.	NA
21	RFIU3	JTAG TDO. Left unconnected.	NA
22	RFIU4	JTAG TMS. Connect to GND through a 1K resistor.	NA

23	RFIU5	JTAG TDI. Connect to GND through a 1K resistor.	NA
24	VSSIO	Ground reference for IO pins.	S
25	VDDIO	Positive supply for IO pins. Connect to 3.3V supply.	S
26	VDD	Positive supply for logic. Connect to 1.2V supply.	S
27	VSS	Ground reference for logic.	S
28	RFIU6	JTAG TCK. Connect to GND through a 1K resistor	NA
29	RFIU7	JTAG TRST. Connect to GND through a 1K resistor	NA
30	RFIU8	Test mode select. Connect to GND through a 1K resistor.	NA
31	I2C_SDA2	I2C 2 Serial Data.	I/O
32	I2C_SCL2	I2C 2 Serial Clock.	I/O
33	I2C_SCL0	I2C 0 Serial Clock.	I/O
34	I2C_SDA0	I2C 0 Serial Data.	I/O
35	VSS	Ground reference for logic.	S
36	VDD	Positive supply for logic. Connect to 1.2V supply.	S
37	VDDIO	Positive supply for IO pins. Connect to 3.3V supply.	S
38	VSSIO	Ground reference for IO pins.	S
39	SPI_SS1	SPI 1 Chip Select.	O
40	SPI_SCLK1	SPI 1 Clock.	O
41	SPI_MISO1	SPI 1 Master In Slave Out.	I
42	SPI_MOSI1	SPI 1 Master Out Slave In.	O
43	PUSH_RESETN	Reset. (ACTIVE LOW)	I
44	CLK	System Clock.	I
45	UART_TX1	UART 1 Serial Out / Transmit.	O
46	VDDIO	Positive supply for IO pins. Connect to 3.3V supply.	S

47	VSSIO	Ground reference for IO pins.	S
48	VSS	Ground reference for logic.	S
49	VDD	Positive supply for logic. Connect to 1.2V supply.	S
50	UART_RX1	UART 1 Serial In / Receive.	I
51	GPIO15	General purpose IO GPIO0(15).	I/O
52	GPIO14	General purpose IO GPIO0(14).	I/O
53	GPIO13	General purpose IO GPIO0(13).	I/O
54	GPIO12	General purpose IO GPIO0(12).	I/O
55	GPIO11	General purpose IO GPIO0(11).	I/O
56	VSS	Ground reference for logic.	S
57	VDD	Positive supply for logic. Connect to 1.2V supply.	S
58	GPIO10	General purpose IO GPIO0(10).	I/O
59	VDDIO	Positive supply for IO pins. Connect to 3.3V supply.	S
60	VSSIO	Ground reference for IO pins.	S
61	GPIO9	General purpose IO GPIO0(9).	I/O
62	GPIO8	General purpose IO GPIO0(8).	I/O
63	GPIO7	General purpose IO GPIO0(7).	I/O
64	GPIO6	General purpose IO GPIO0(6).	I/O
65	GPIO5	General purpose IO GPIO0(5).	I/O
66	GPIO4	General purpose IO GPIO0(4).	I/O
67	VSS	Ground reference for logic.	S
68	VDD	Positive supply for logic. Connect to 1.2V supply.	S
69	VDDIO	Positive supply for IO pins. Connect to 3.3V supply.	S
70	VSSIO	Ground reference for IO pins.	S

71	GPIO3	General purpose IO GPIO0(3).	I/O
72	GPIO2	General purpose IO GPIO0(2).	I/O
73	GPIO1	General purpose IO GPIO0(1).	I/O
74	GPIO0	General purpose IO GPIO0(0).	I/O
75	PWM_7	Pulse Width Modulation.	O
76	PWM_6	Pulse Width Modulation.	O
77	PWM_5	Pulse Width Modulation.	O
78	VSS	Ground reference for logic.	S
79	VDD	Positive supply for logic. Connect to 1.2V supply.	S
80	PWM_4	Pulse Width Modulation.	O
81	PWM_3	Pulse Width Modulation.	O
82	PWM_2	Pulse Width Modulation.	O
83	VDDIO	Positive supply for IO pins. Connect to 3.3V supply.	S
84	VSSIO	Ground reference for IO pins.	S
85	PWM_1	Pulse Width Modulation.	O
86	PWM_0	Pulse Width Modulation.	O
87	SPI_MOSI0	SPI 0 Master Out Slave In.	O
88	VSS	Ground reference for logic.	S
89	VDD	Positive supply for logic. Connect to 1.2V supply.	S
90	SPI_MISO0	SPI 0 Master In Slave Out.	I
91	SPI_SCLK0	SPI 0 Clock.	O
92	SPI_SS0	SPI 0 Chip Select.	O
93	VDDIO	Positive supply for IO pins. Connect to 3.3V supply.	S
94	VSSIO	Ground reference for IO pins.	S

95	I2C_SDA1	I2C 1 Serial Data.	I/O
96	I2C_SCL1	I2C 1 Serial Clock.	I/O
97	SPI_MOSI2	SPI 2 Master Out Slave In.	O
98	SPI _MISO2	SPI 2 Master In Slave Out.	I
99	VDD	Positive supply for logic. Connect to 1.2V supply.	S
100	VSS	Ground reference for logic.	S
101	SPI_SCLK2	SPI 2 Clock.	O
102	SPI_SS2	SPI 2 Chip Select.	O
103	VSSIO	Ground reference for IO pins.	S
104	VDDIO	Positive supply for IO pins. Connect to 3.3V supply.	S
105	UART_RX2	UART 2 Serial In / Receive.	I
106	UART_TX2	UART 2 Serial Out / Transmit.	O
107	UART_RX0	UART 0 Serial In / Receive.	I
108	UART_TX0	UART 0 Serial Out / Transmit.	O
109	GPIO31	General purpose IO GPIO1(15).	I/O
110	GPIO30	General purpose IO GPIO1(14).	I/O
111	GPIO29	General purpose IO GPIO1(13).	I/O
112	VDD	Positive supply for logic. Connect to 1.2V supply.	S
113	VSS	Ground reference for logic.	S
114	VSSIO	Ground reference for IO pins.	S
115	VDDIO	Positive supply for IO pins. Connect to 3.3V supply.	S
116	GPIO28	General purpose IO GPIO1(12).	I/O
117	GPIO27	General purpose IO GPIO1(11).	I/O
118	GPIO26	General purpose IO GPIO1(10).	I/O

119	GPIO25	General purpose IO GPIO1(9).	I/O
120	GPIO24	General purpose IO GPIO1(8).	I/O
121	GPIO23	General purpose IO GPIO1(7).	I/O
122	GPIO22	General purpose IO GPIO1(6).	I/O
123	VSSIO	Ground reference for IO pins.	S
124	VDDIO	Positive supply for IO pins. Connect to 3.3V supply.	S
125	VDD	Positive supply for logic. Connect to 1.2V supply.	S
126	VSS	Ground reference for logic.	S
127	GPIO21	General purpose IO GPIO1(5).	I/O
128	GPIO20	General purpose IO GPIO1(4).	I/O

S- Supply, I/O - Input/Output, I - Input, O - Output, RFIU - Reserved for internal use

4. Memory mapping

Table 4. THEJAS32 SoC memory map

Peripheral	Start Address	End Address	Interrupt Number
SRAM	0x0020_0000	0x0023_ffff	
UART 0	0x1000_0100	0x1000_01FF	0
UART 1	0x1000_0200	0x1000_02FF	1
UART 2	0x1000_0300	0x1000_03FF	2
SPI 0	0x1000_0600	0x1000_06FF	3
SPI 1	0x1000_0700	0x1000_07FF	4
I2C 0	0x1000_0800	0x1000_08FF	5
I2C 1	0x1000_0900	0x1000_09FF	6
TIMER 0	0x1000_0A00	0x1000_0A10	7
TIMER 1	0x1000_0A14	0x1000_0A24	8
TIMER 2	0x1000_0A28	0x1000_0A38	9
TIMERSINTSTATUS	0x1000_0AA0		
TIMERSEOI	0x1000_0AA4		
TIMERSRAWINT STATUS	0x1000_0AA8		
I2C 2	0x1000_1000	0x1000_1FFF	
GPIO	0x1008_0000	0x101C_0000	10-22
SPI 2	0x1020_0100	0x1020_01FF	23
PWM	0x1040_0000	0x1040_00FF	24 - 31
PLIC	0x2001_0000	0x2001_FFFF	

5. Electrical characteristics

5.1. Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 5: current characteristics and Table 6: voltage characteristics cause permanent device damage if this absolute rating exceeds even for a very short period of time.

Table 5. Current characterstics

Symbols	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source)	95	mA
I_{VSS}	Total current out of VSS ground lines (sink)	95	
I_{IO} (DC Current per I/O Pin)	Output current sunk by PROC_HB, GPIO0, GPIO1, SPI 0, SPI 1, SPI3, SPI 3	12	
	Output current source by PROC_HB, GPIO0, GPIO1, SPI 0, SPI 1, SPI3, SPI 3	12	
	Output current sunk by I2C 0, I2C 1, I2C 2, PWM, UART 0, UART 1, UART 2	8	
	Output current source by I2C 0, I2C 1, I2C 2, PWM, UART 0, UART 1, UART 2	8	

Table 6. Voltage characterstics

Symbol	Parameter	Rating	Units
VDD	Device Supply Voltage(1.2V Core Voltage)	1.5	V
VDDIO	Device IO Supply Voltage	3.9	V

Temperature range	Operating temperature	70	°C

5.2. Operating conditions

5.2.1. General operating conditions

Table 7. General operating conditions

Symbol	parameter	Min	Nom	Max	Units
VDD	Device Supply Voltage(1.2V Core Voltage)	1.08	1.2	1.32	V
VDDIO	Device IO Supply Voltage	2.97	3.3	3.63	V
Temp	Operating Temperature range	0	+25	+70	°C

5.2.2. Absolute maximum ratings (electrical sensitivity)

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 8. ESD ratings

Symbol	Ratings	Conditions	Class	Maximum value	Unit
VESD(HBM)	Electrostatic discharge voltage (human body model)	TA = +25 °C conforming to JESD22-A114	2	2000	V

VESD(CDM)	Electrostatic discharge voltage (charge device model)	TA = +25 °C conforming to JESD22-C101	II	500	V
VESD(MM)	Electrostatic discharge voltage (Machine model)			200	v

5.2.3. I/O port characteristics

Table 9. Input voltage characteristics

Symbol	Parameter	Min	Nom	Max	Units
V_{IH}	High Level Input Voltage	2		VDDIO+0.3	V
V_{IL}	Low Level Input Voltage			0.4	V

Table 10. Output voltage characteristics

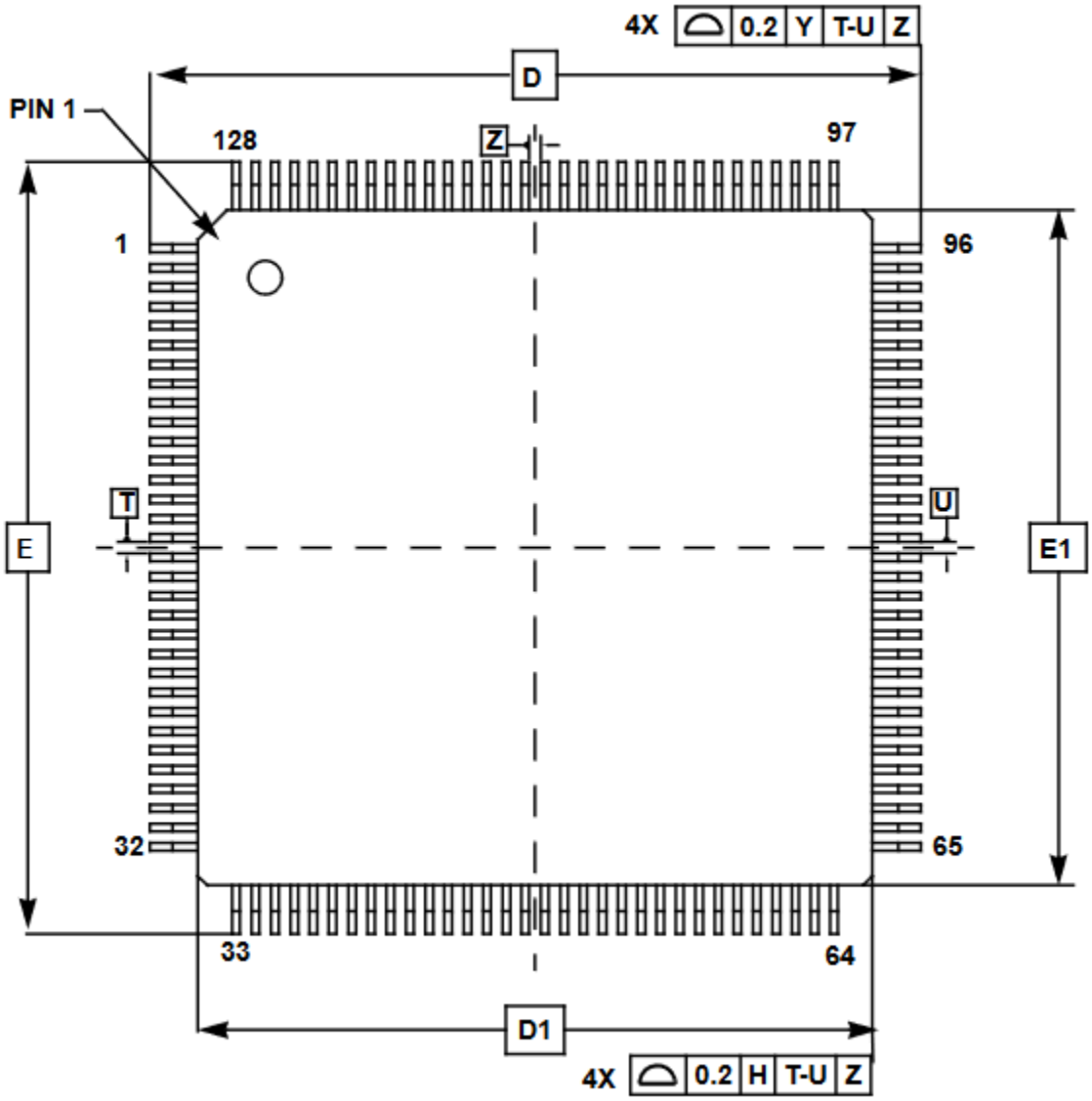
Symbol	Parameter	Min	Nom	Max	Units
V_{OH}	High Level Output Voltage	2.4			V
V_{OL}	Low Level Output Voltage			0.8	V
V_{OH}	High Level Output Voltage IOH = 100uA	0.8*VDDIO			V
V_{OL}	Low Level Output Voltage IOH			0.2*VDDIO	V

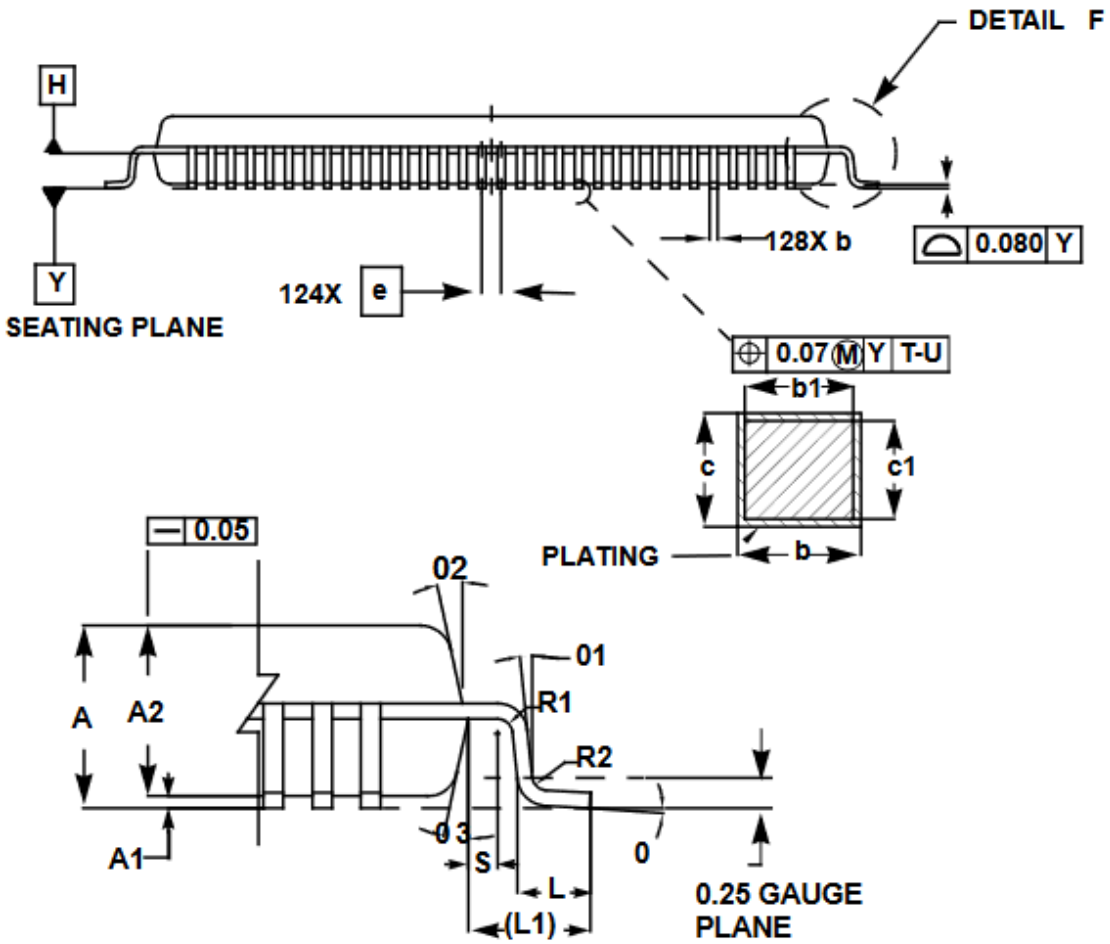
	= 100uA				
VSLEW[2]	Output slew rate(fast slew rate)		4		
	Output slew rate(medium slew rate)		2		

6. Package information

The mechanical details for the THEJAS32 SoC in the LQFP128 package are provided below.

Figure 12. LQFP128 - 128-pin, 14 x 14 mm low-profile quad flat package outline




DETAIL F
H
Y
SEATING PLANE
124X
e
128X b
0.080 Y
0.07 M Y T-U
b1
c
c1
PLATING
b
0.05
02
01
R1
R2
A
A2
A1
03
S
L
(L1)
0
0.25 GAUGE
PLANE

DETAIL F

Table 11. THEJAS32 SoC Dimension in mm

SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	-		1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.13		0.23
c	0.09		0.20
D	16 BSC		
D1	14 BSC		
E	16 BSC		
E1	14 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
0	0°	3.5°	7°
e	0.40 BSC		

NOTES:-

- Dimensions are in millimeters.
- Dimensions D1 and E1 are excluding mold protrusion. Allowable protrusion is 0.25 per side. Dimensions D1 and E1 are exclusive of mold mismatch and determined by datum plane H.
- Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located at the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

7. Revision history

Table 12. Document revision history

Date	Revision	Changes
15/12/2023	v 1.0	Initial release